REMARKS

These remarks are responsive to the Office Action mailed January 25, 2008 ("Office Action").

STATUS OF THE CLAIMS

Claims 1-24 are currently pending in the present application, with claims 1 and 10 being the independent claims. Claim 24 is a newly added claims.

35 USC § 103(a)

The Office Action rejects claims 1-23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,515,826 to Hsiao et al. (Hsiao) in view U.S. Pat. No. 6,242,320 to So (So), and further in view of Hartmannsgruber, et al., "A Selective CMP Process for Stacked low-k'CVD Oxide Films", Microelectronic Engineering, Vol. 50, pg. 53-58, 2000 (Hartmannsgruber).

Under item 5 of the Office Action, the Examiner alleges that Hsiao discloses and shows a device and a method of manufacturing a semiconductor structure utilizing aspect ratio dependent etching, comprising:

a. forming a test structure, defined by a systematic row of a plurality of trenches having different widths and different depths in a defined manner, in an active wafer 300, said wafer receiving an active circuit 148 in a later stage.

As discussed in the response to the non-final office action, Hsiao does not refer to forming the test structure having the systematic row of trenches **in an active wafer**, wherein the same wafer receives an active circuit in a later manufacturing step as is recited in claim 1 as presently on file (last group of features). Nowhere in the description relating to Figs. 15 and 16 of Hsiao is there a disclosure of anything that could be alleged to be a three layer test structure, i.e., the alumina etch stop layer, the layer of etchable material, such as polymer or SiO_2, and the etch mask are formed on actual product carrier materials, as is submitted by the Examiner.

Rather, it appears that Hsiao discloses to use an etch mask having two types of openings in the etch mask (cf. column 7, line 22 onward), i.e., relatively wide openings for electrical

interconnects and relatively narrow openings for the induction coil. Moreover, in the description of Fig. 16, it is explicitly referred to the test structure of Figure 15 formed by using a specified etch time T1, while an additional etch time T2 is also referred to that illustrates the differences in etch depth after a long etch process time, col. 7, lines 35 to 40 and col. 3, line 7. From these test data appropriate etch process parameters may be selected for etching **an insulating material layer** in actual product substrates to reliably etch through the entire insulating material for the interconnects while reliably maintaining residual insulating material for the induction coil openings.

Thus, the insulating material 300 of Hsiao does not represent an active wafer, nor does this document teach or suggest using the "active wafer" including the test structure for forming an active circuit.

Under item 5, the Examiner alleges further that:

> b. wherein a targeted thickness of the active wafer during the removal corresponds to a depth of a reference trench of the trenches of the test structure, said reference trench being flanked by shallower and deeper trenches, in particular by a neighboring shallower and a neighboring deeper trench.

Also in this case, "a targeted thickness of the active wafer during the removal" in the context of the test structure is not disclosed by Hsiao. Rather, it appears that the "removal process. in Hsiao could only be understood as the etch process for forming openings in the insulating material of the test structure or the inductive coil layer. In both cases the thickness of the insulating material layer is maintained constant.

Case (a): In the actual products only two types of openings are provided, that is, the interconnect openings, extending fully through the insulating material, and the induction coil openings extending to a certain depth. Hence in this case, irrespective of the fact that the insulating material layer does not represent an active wafer, the interconnect opening may be considered as reference trench, which would, however, not be flanked by a shallower and a deeper trench (see third group of features). On the other hand, the induction coil opening may be considered as the reference trench and in this case, the depth thereof would not correspond to the "thickness of the active wafer" – even if one were to consider the insulating material layer as the active wafer – and this reference trench would also not be flanked by a shallower and deeper trench.

Case (b): In the test structure shown in Figure 15 only the trenches 332 and 336 correspond to the (constant) thickness of the insulating material layer. However, these trenches are not flanked by shallower and deeper trenches. If any other trench is considered as reference, such as trench 350 (with respect to etch time T1), as is the case in the Office Action, this trench would be flanked by shallower and deeper trenches; however, the depth thereof would not correspond to the thickness of the insulating material and would certainly not correspond to the thickness of the active wafer.

Consequently, Hsiao fails to disclose at least the above indicated features. Moreover, as already pointed out in our previous response, the test structure of Hsiao only refers to the **pattern dependent etch process** so as to select appropriate etch parameters of forming interconnect openings and induction coil openings in a single etch step in actual product substrates. No indication whatsoever may be obtained from Hsiao with respect to monitoring a thickness reduction of an active wafer on the basis of a systematic row of trenches formed therein during the removal of material from the active wafer. We claim a method doing so. Hsiao does not disclose such method for monitoring.

Under item 7 of the Office Action, the Examiner alleges that So discloses:

c. forming a structure in an active wafer ... with a plurality of different trenches with different depths including a reference trench;
d. performing the wafer material removal process comprising a polishing process...
e. bonding the active wafer ... onto the second wafer ...;
f. forming an active circuit in said active wafer in the later step.

Under items 8 and 9 the Examiner then concludes that it would have been obvious for the skilled person – in view of having a **uniform semiconductor layer** in the active wafer, **enhanced surface conditions** for the device to be formed and for overall **improved device characteristics** – to modify Hsiao by incorporating steps (c) to (f) of So. However, in view of the advantages cited above that are to be gained in forming SOI devices, the combination of the teachings does not provide a method as described in the present claims. That is, even if the above cited documents were to be combined in view of the advantages to be gained – which we argue is not the case – additional inventive skill would be required (under the KSR test) so as to arrive at the solution of claim 1. For example, Hsiao and So both fail to disclose how to provide

the trenches of different depths in the active wafer so that a targeted thickness of the active wafer corresponds to the depth **of a reference trench**, optically detected.

As discussed above, Hsiao fails to teach or suggest a respective reference trench flanked by a shallower and a deeper trench, wherein the depth of the reference trench corresponds to the targeted thickness of the active wafer. So teaches a first type of isolation trenches of a first reduced depth and a specified width and a second type of trenches o a second increased thickness and having the same specified width that are considered as reference trenches by the Examiner. However, the "reference" trenches of So are not flanked by shallower and deeper trenches as is presently claimed to obtain superior process control during the **material removal process** of the active wafer. This is a different method, which is not obvious from the prior art.

Hence, for at least these reasons and also supplemented by the additional feature of optically detecting the exposure of the reference trench, which is not disclosed by either Hsiao or So, a hypothetical combination of these documents does not render claim 1 obvious. Assuming, *arguendo*, that these documents may be combined with Hartmannsgruber, the method of claim 1 is not obvious in view of these teachings, as at least the above the specified feature is not disclosed in any of these documents; that is, a reference trench having a depth corresponding to the target thickness of the active semiconductor layer and flanked by both a shallower and a deeper trench. This is highly efficient for optically detecting the progress of the polishing process and providing for enhanced flexibility of selecting a desired target thickness on the basis of the same test structure configuration.

Similar arguments apply to device claim 10, which refers to an SOI structure including a test structure and active circuits, thereby allowing to perform the method discussed above.

An indication of allowance of all claims is respectfully requested.

CONCLUSION

Pursuant to 37 CFR § 1.136(a), Applicant hereby petitions for a One-Month Extension of Time. Commissioner is hereby authorized to charge fees in the amount of **$120.00** as set forth under 37 CFR § 1.136(a) for the One-Month Extension of Time, to include responding up through May 27, 2008. In the event any variance exist, the Commissioner is hereby authorized to debit or credit undersigned's Deposit Account No. 50-0206 to cure any such underpayments or overpayments of fees as required.

A notice of allowance is earnestly solicited.

Respectfully submitted,

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